Using Status Registers

A wide range of status registers allows the LSA1000's internal processing status to be determined quickly at any time. These registers and the instrument's status reporting system are designed to comply with IEEE 488.2 recommendations. *Following an overview, starting this page, each of the registers and their roles are described.*

Related functions are grouped together in common status registers. Some, such as the Status Byte Register (STB) or the Standard Event Status Register (ESR), are required by the IEEE 488.2 Standard. Other registers are device-specific, and include the Command Error Register (CMR) and Execution Error Register (EXR). Those commands associated with IEEE 488.2 mandatory status registers are preceded by an asterisk <*>.

Overview

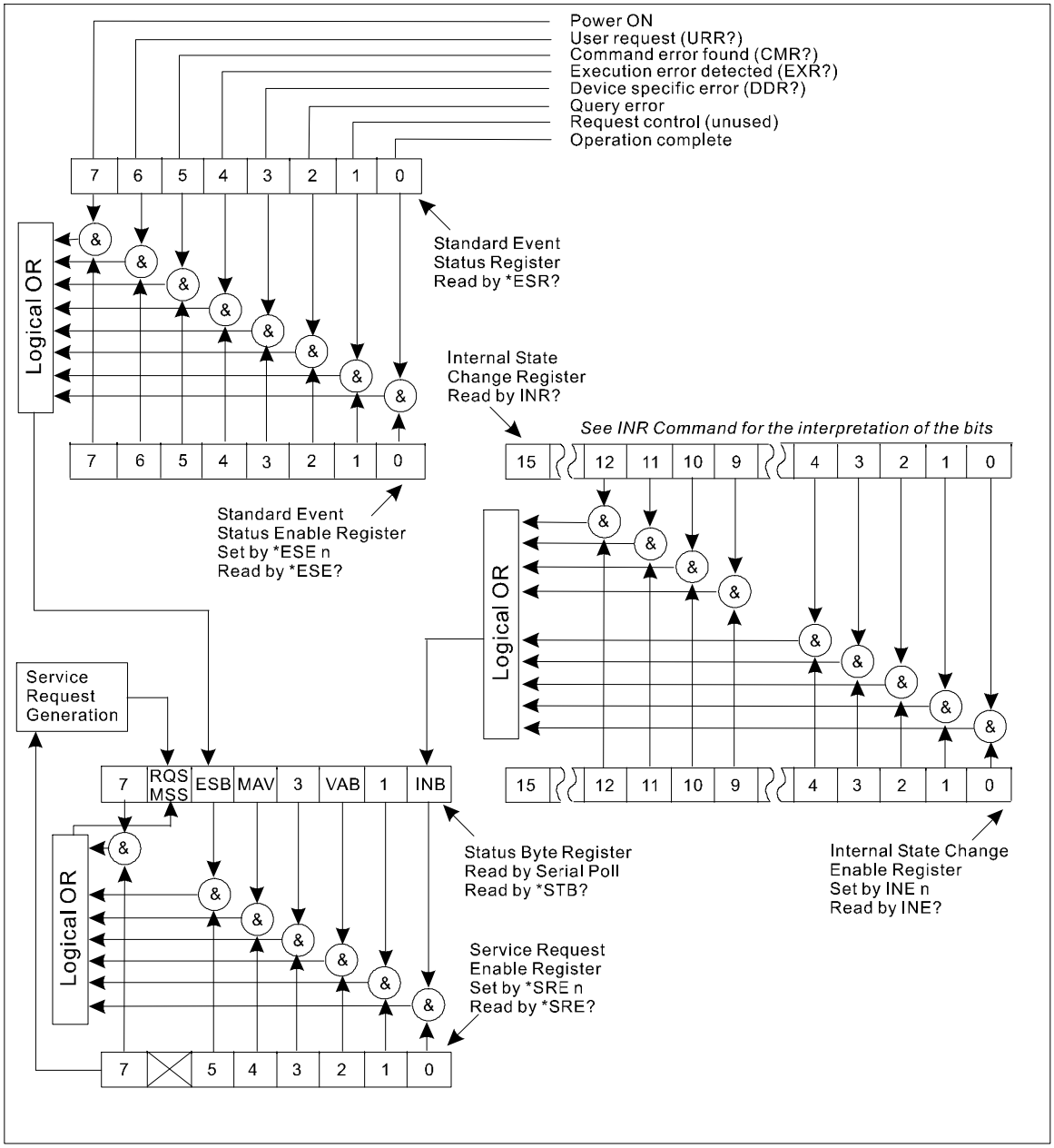
The Standard Event Status Bit (ESB) and the Internal Status Change Bit (INB) in the Status Byte Register are summary bits of the Standard Event Status Register (ESR) and the Internal State Change Register (INR). The Message Available Bit (MAV) is set whenever there are data bytes in the output queue. The Value Adapted Bit (VAB) indicates that a parameter value was adapted during a previous command interpretation (for example, if the command "TDIV 2.5 US" is received, the timebase is set to 2 µs/div along with the VAB bit).

The Master Summary Status bit (MSS) indicates a request for service from the instrument. The MSS bit can only be set if one or more of the other bits of STB are enabled with the Service Request Enable Register (SRE).

All Enable registers (SRE, ESE and INE) are used to generate a bit-wise AND with their associated status registers. The logical OR of this operation is reported to the STB register. At power-on, all Enable registers are zero, inhibiting any reporting to the STB.

The Standard Event Status Register (ESR) primarily summarizes errors, whereas the Internal State Change Register (INR) reports internal changes to the instrument. Additional

details of errors reported by ESR can be obtained with the queries “CMR?”, “DDR?” and “EXR?”.



Status Register Structure

The register structure contains one additional register, not shown in the figure on the previous page. This is the Parallel Poll Enable Register (PRE), which behaves exactly like the Service Request Enable Register (SRE), but sets the “ist” bit (also not shown in the figure), used in the Parallel Poll. The “ist” bit can also be read with the “*IST?” query.

Example

If an erroneous remote command — “TRIG_MAKE SINGLE”, for example — is transmitted to the instrument, it rejects the command and sets the Command Error Register (CMR) to the value 1 (unrecognized command/query header). The non-zero value of CMR is reported to Bit 5 of the Standard Event Status Register (ESR), which is then set.

Nothing further occurs unless the corresponding Bit 5 of the Standard Event Status Enable Register (ESE) is set (with the command “*ESE 32”), enabling Bit 5 of ESR to be set for reporting to the summary bit ESB of the Status Byte Register (STB).

If setting of the ESB summary bit in STB is enabled, again nothing occurs unless further reporting is enabled by setting the corresponding bit in the Service Request Enable Register (with the command “*SRE 32”). In this case, the generation of a non-zero value of CMR ripples through to the Master Summary Status bit (MSS), generating a Service Request (SRQ).

The value of CMR can be read and simultaneously reset to zero at any time with the command “CMR?”. The occurrence of a command error can also be detected by analyzing the response to “*ESR?”. However, if several types of potential errors must be surveyed, it is usually far more efficient to enable propagation of the errors of interest into the STB with the enable registers ESE and INE.

Summary

A command error (CMR) sets Bit 5 of ESR if:

- Bit 5 of ESE is set, ESB of STB is also set, or
- Bit 5 of SRE is set, MSS/RQS of STB is also set and a Service Request is generated.

Status Byte Register (STB)

The Status Byte Register (STB) is the instrument's central reporting structure. The STB is composed of eight single-bit summary messages (of which three are unused), which reflect the current status of the associated data structures implemented in the instrument:

- **Bit 0** is the summary bit INB of the Internal State Change Register. It is set if any of the bits of the INR are set, provided they are enabled by the corresponding bit of the INE register.
- **Bit 2** is the Value Adapted bit, indicating that a parameter value was adapted during a previous command interpretation.
- **Bit 4** is the Message Available (MAV) bit, indicating that the interface output queue is not empty.
- **Bit 5** is the summary bit ESB of the Standard Event Status Register. It is set if any of the bits of the ESR are set, provided they are enabled by the corresponding bit of the ESE register.
- **Bit 6** is either the Master Summary Status bit (MSS) or the Request for Service bit (RQS), owing to the STB being able to be read in two different ways. The command "*STB?" reads and clears the STB in the query mode, in which case Bit 6 is the MSS bit, and indicates whether the instrument has any reason for requesting service.

The Status Byte Register can be read using the query "*STB?". The response represents the binary weighted sum of the register bits. The register is cleared by "*STB?", "ALST?", "*CLS", or after the instrument has been powered up.

Another way of reading the STB is using the serial poll (*see "Instrument Polls", Chapter 3*). In this case, Bit 6 is the RQS bit, indicating that the instrument has activated the SRQ line on the GPIB. The serial poll only clears the RQS bit. Therefore, the MSS bit of the STB (and any other bits which caused MSS to be set) will stay set after a serial poll. These bits must be reset.

Standard Event Status Register (ESR)

The Standard Event Status Register (ESR) is a 16-bit register reflecting the occurrence of events. The ESR bit assignments have been standardized by IEEE 488.2. Only the lower eight bits are currently in use.

The ESR is read using the query “*ESR?”. The response is the binary weighted sum of the register bits. The register is cleared with an “*ESR?” or “ALST?” query, a “*CLS” command or after power-on.

Example

The response message “*ESR 160” indicates that a command error occurred and that the ESR is being read for the first time after power-on. The value 160 can be broken down into 128 (Bit 7) plus 32 (bit 5). *See the table on the same page as the ESR command description for the conditions corresponding to the bits set.*

The “Power ON” bit appears only on the first “*ESR?” query after power-on because the query clears the register. This type of command error can be determined by reading the Command Error Status Register with the query “CMR?”. Note that it is not necessary to read (nor simultaneously clear) this register in order to set the CMR bit in the ESR on the next command error.

Standard Event Status Enable Register (ESE)

The Standard Event Status Enable Register (ESE) allows one or more events in the Standard Event Status Register to be reported to the ESB summary bit in the STB.

The ESE is modified with the command “*ESE” and cleared with the command “*ESE 0”, or after power-on. It is read with the query “*ESE?”.

Example

“*ESE 4” sets bit 2 (binary 4) of the ESE Register, enabling query errors to be reported.

Service Request Enable Register (SRE)

The Service Request Enable Register (SRE) specifies which summary bit(s) in the Status Byte Register will bring about a service request. The SRE consists of eight bits. Setting a bit in this register allows the summary bit located at the same bit position in the Status Byte Register to generate a service request, provided that the associated event becomes true. Bit 6 (MSS) cannot be set and is always reported as zero in response to the query “*SRE?”.

SRE is modified with the command "*SRE" and cleared with the command "*SRE 0", or after power-on. It may be read with the query "*SRE?".

Parallel Poll Enable Register (PRE)

The Parallel Poll Enable Register (PRE) specifies which summary bit(s) in the Status Byte Register will set the "ist" individual local message. This register is quite similar to the Service Request Enable Register (SRE), but is used to set the parallel poll "ist" bit rather than MSS.

The value of the "ist" may also be read without a Parallel Poll via the query "*IST?". The response indicates whether or not the "ist" message has been set (values are 1 or 0).

The PRE is modified with the command "*PRE" and cleared with the command "*PRE 0", or after power-on. It is read with the query "*PRE?". (*See Chapter 3 "Instrument Polls".*)

Example

"*PRE 5" sets bits 2 and 0 (decimal 4 and 1) of the Parallel Poll Enable Register.

Internal State Change Status Register (INR)

The Internal State Change Status Register (INR) reports the completion of a number of internal operations (*the events tracked by this 16-bit-wide register are listed with the "INR?" query in the System Commands section*).

The INR is read using the query "INR?". The response is the binary-weighted sum of the register bits. The register is cleared with an "INR?" or "ALST?" query, a "*CLS" command, or after power-on.

Internal State Change Enable Register (INE)

The Internal State Change (INE) allows one or more events in the Internal State Change Status Register to be reported to the INB summary bit in the STB.

The INE is modified with the command "INE" and cleared with the command "INE 0", or after power-on. It is read with the query "INE?".

Command Error Status Register (CMR)

The Command Error Status register contains the code of the last command error detected by the instrument. Command error codes are listed with the command "CMR?".

The Command Error Status Register may be read using the query "CMR?". The response is the error code. The register is cleared with a "CMR?" or "ALST?" query, a "*CLS" command, or after power-on.

Device Dependent Error Status Register (DDR)

The Device Dependent Error Status Register (DDR) indicates the type of hardware errors affecting the instrument. Individual bits in this register report specific hardware failures. They are listed with the command “DDR?”.

The DDR is read using the “DDR?” query. The response is the binary weighted sum of the error bits. The register is cleared with a “DDR?” or “ALST?” query, a “*CLS” command, or after power-on.

Execution Error Status Register (EXR)

The Execution Error Status Register (EXR) contains the code of the last execution error detected by the instrument. Execution error codes are listed with the command “EXR?”.

The EXR is read using the “EXR?” query. The response is the error code. The register is cleared with an “EXR?” or “ALST?” query, a “*CLS” command, or after power-on.

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